ENERGY AND RADIO SCIENCE

Autonomous DC-DC Converter for RF energy Harvesting

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Abstract
This article presents a DC-DC converter topology suitable for ultra-low power and low voltage applications. The presented topology is dedicated to energy harvesting sources in general and especially for Radio-Frequency RF sources. Main advantage of this converter is its autonomy, i.e., it operates from low voltage levels without the need of an external energy source or any other startup assistances. Theoretical modelling of the converter is used together with circuit simulations in order to make an optimal design based on the requirements of a low power rectifying antenna (rectenna). A discrete prototype was fabricated and tested.

Introduction
Wireless sensors networks (WSNs) are nowadays ubiquitous in various kinds of applications like: monitoring and control, smart building, healthcare, etc. The expansion of WSNs is due, among other reasons, to the efforts made by designers in order to develop low-power circuits. Though those circuits are optimized for low-power and have excellent power budget, the problem of autonomy is still there. In fact, the performances required from an autonomous sensor grow day by day and it is likewise for power consumption. In most applications, batteries are used alone in order to supply WSN's nodes. In this case, the sensor life-time is limited. So, designers begin to use energy harvesting as a support together with batteries. Harvested energy could be used to recharge the batteries or/and to power directly the sensors. In most cases, energy harvesting sources deliver very low voltage level (<1V). However, a level of some volts is needed in order to be able to power conventional circuits as autonomous sensors. Power management system based on step-up DC-DC converter is used for this purpose.
In this paper a start-up converter based on the Armstrong oscillator is used in order to improve the DC voltage sensitivity. A flyback converter operating in discontinuous conduction mode (DCM) is used to match the output impedance of the rectenna in order to extract the maximum available power. A normally-on P-channel JFET is connected to the low-side of the start-up converter allowing to switch it off once the Flyback is operating. An Under-voltage lock-out (UVLO) circuit is proposed to manage the operation of the load as function of the available power from the source (figure 1).

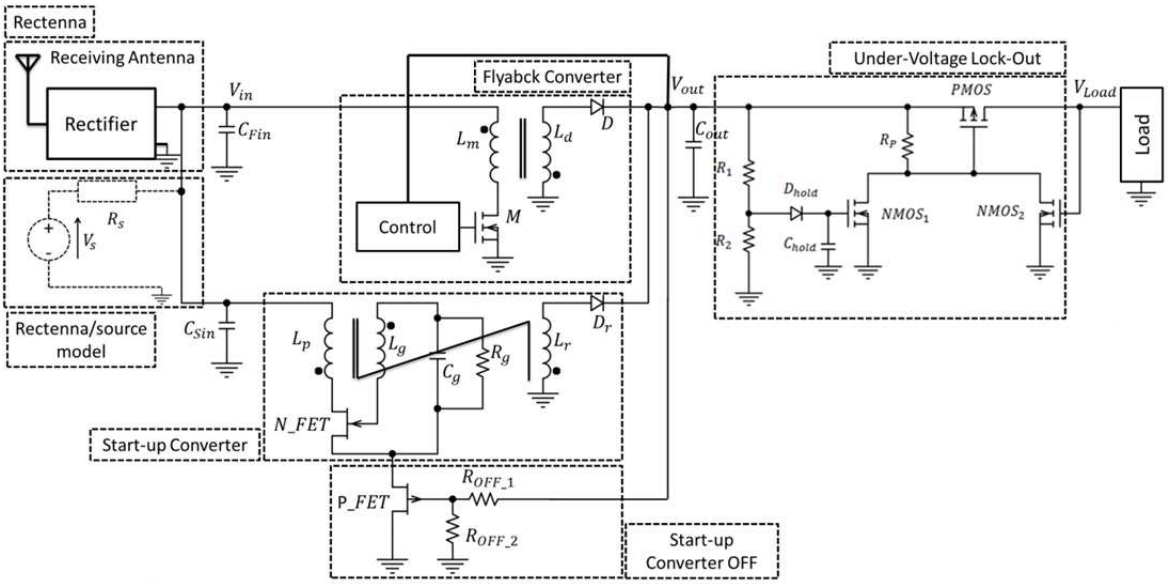

Figure 1: Topology of power management system for low power rectenna

1. Rectenna for RF energy Harvesting

A rectenna is composed by an antenna and a rectifier. For low power UHF applications the rectifier is very often realized using Schottky diodes thanks to their low threshold voltage and low junction capacitance. A band-pass filter is used between the antenna and the rectifier in order to realize impedance matching for the working frequency. This allows also to avoid high frequency harmonics from the rectifier to be radiated back by the antenna. The output filter is a low-pass filter which allows to cut-off high frequency harmonics from the rectifier [1].
A specific rectenna has been experimentally tested in anechoic chamber with different levels of RF power P_{RF} (at 2.45 GHz: Wifi frequency) over a wide range of DC resistive load R_L [2, 3]. The DC voltage V_{dc} provided by the rectenna has been measured and the RF/DC power conversion efficiency $\eta_{RF/DC}$ has then been evaluated as follow:

$$\eta_{RF/DC} = \frac{P_{dc\_rect}}{P_{RF}} = \frac{\frac{V_{dc\_rect}^2}{R_L}}{P_{RF}} \quad (1)$$

Current-voltage characteristics are almost parallel straight lines (figure 2). The rectenna can then be modeled as a DC voltage source in series with resistive impedance. Also, as current-voltage characteristics are parallel, the rectenna impedance is almost constant over a wide range of RF power levels. The characteristics of efficiency confirm this deduction as the efficiency is maximal for a specific value of the output load. This optimal load Rs (related to maximum efficiency) decreases slightly when RF power increases: Rs = 1200 Ω at -20 dBm and Rs = 800 Ω at -8 dBm. Note that the ambient RF energy available depends on the place where the system is placed and on the surface of the antenna. But we can imagine that it is possible to collect a power of -20 dBm with an adapted antenna.

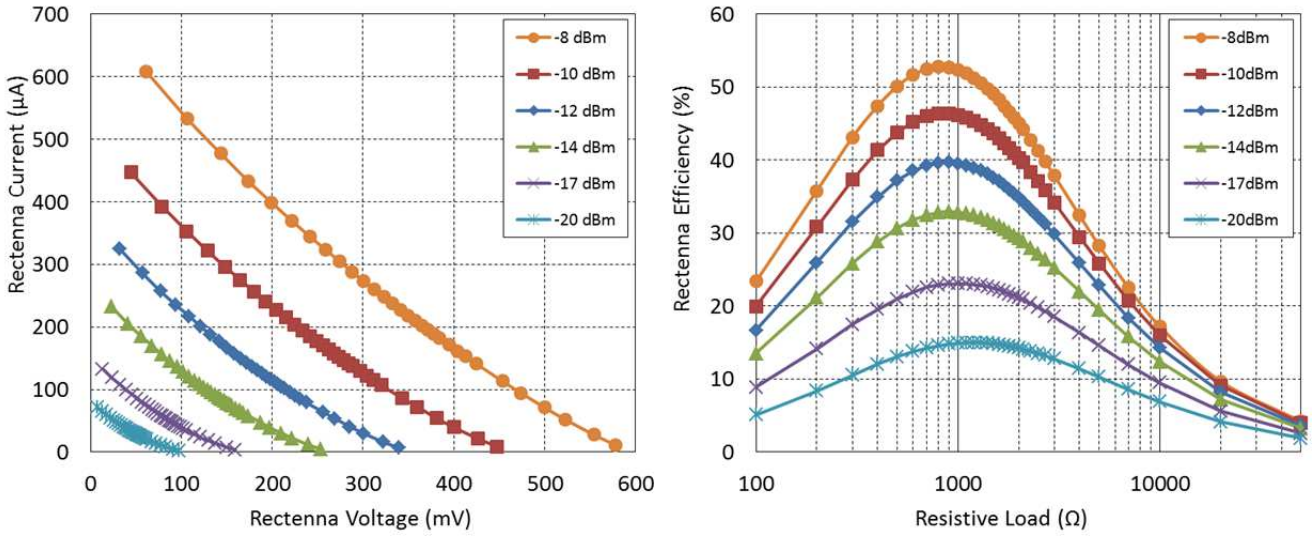

Figure 2: Rectenna characteristics for different RF power levels: Current-Voltage (left) and RF/DC Efficiency-Load (right).

2. Autonomy: start-up converter

DC/DC Converters need in general either an auxiliary power supply or a sufficiently high input source voltage in order to operate properly. As these two possibilities are absent in our application, a specific converter topology based on the Armstrong oscillator is presented.

2.1. Armstrong-Oscillator converter

The Armstrong oscillator is a harmonic oscillator able to exhibit high oscillation levels from very low DC voltage [4, 5, 6]. That way, very-low operation voltage could be achieved. The classic version uses only a two winding transformer and the inherent gate-source diode of the JFET for rectification. So, the output DC voltage is inversed as regard to the source one. This paper presents a more advanced topology which uses a ternary winding associated with a separate rectification diode. The output is then isolated from the source and can be arranged as desired.
As shown at Figure 1 the converter topology is mainly composed by two components: a transformer and a normally-on N-channel JFET. The operation of the converter is based on three functional blocks. The first one is the oscillator formed

by the primary side of the transformer and the JFET's gate-source capacitance C_{gs} (resonant cavity) on the one hand, and the JFET (negative gain amplifier) on the other hand. The second function is a voltage step-up thank to the transformer high turn-ratio. A high voltage level is needed at the JFET gate to reach the gate-source cutoff voltage, V_{gs_th}, in order to switch it off ($m_g{}^2 = L_g/L_p$). A high voltage is also needed at the tertiary winding output ($m_r{}^2 = L_r/L_p$) in order to obtain a high DC voltage.
The third functional block is the rectifier, i.e. the diode D_r. As it can be observed from the waveforms in Figure 3, D_r is on when the JFET channel and the JFET inherent gate-source diode, D_{gs}, are conducting. The capacitor C_g is charged negatively when D_{gs} turns on. It allows to obtain a high voltage level at the JFET gate. A high resistor value, R_g, is placed in parallel with C_g in order to stabilize the voltage across this capacitor.

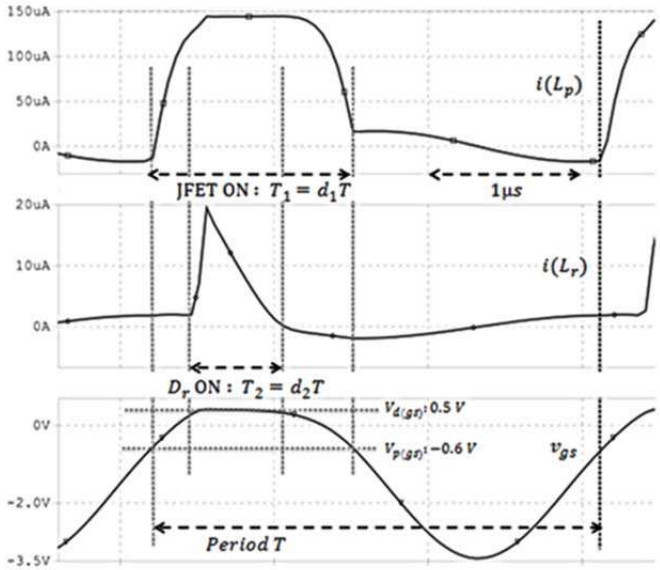

Figure 3: Steady-state simulated waveforms for $V_s = 200\ mV,\ R_s = 1\ k\Omega\ and\ R_{load} = 1\ M\Omega$. Primary inductance current $i(L_p)$, tertiary inductance current $i(L_r)$ and JFET's gate-source voltage, v_{gs}.

A complete theoretical modeling study of the basic Armstrong converter has been reported by the authors in [7]. The small signal model developed for the basic version (two-windings) in [6] stills valid for the converter presented in this paper (three-windings). Consequently, the minimum source start-up voltage $V_{start-up}$ is expressed by the following relationship [7]:

$$V_{start-up} = \frac{2I_{DSS}R_s + |V_{gs\_th}|}{m_g} \tag{2}$$

Where I_{DSS} and V_{gs_th} is the zero-gate-voltage drain current and the channel cutoff voltage of the JFET respectively.

2.2. Experimental tests

A prototype of the three-windings start-up converter was designed and fabricated using discrete components. The best commercially available JFET for our current and voltage ranges is the J201 device (I_{DSS} = 583µA; V_{gs_th} = -0.6V). The tertiary winding rectification diode is a HSMS2822 device which has been chosen thanks to its low forward voltage ($V_f = 340\ mV$) and low leakage (< 30nA at -2.5 V) allowing then to reduce conduction losses. The three windings transformer ($L_p = 50\mu H;\ m_g = 25;\ m_r = 25$) was realized using a compact (20 mm x 10 mm x 6 mm) and high frequency (up to 600 kHz) double E-shape ferrite cores.
The first step in experimental tests was realized using a rectenna emulation model as described at Figure 4. The power conversion efficiency $\eta_{start-up}$ of the converter (Figure 5) has then been evaluated using the following expression:

$$\eta_{start-up} = \frac{P_{start\_out}}{P_{start\_in}} = \frac{\frac{V_{out}^2}{R_{Load}}}{(\frac{V_s - V_{in}}{R_s})V_{in}} \tag{3}$$

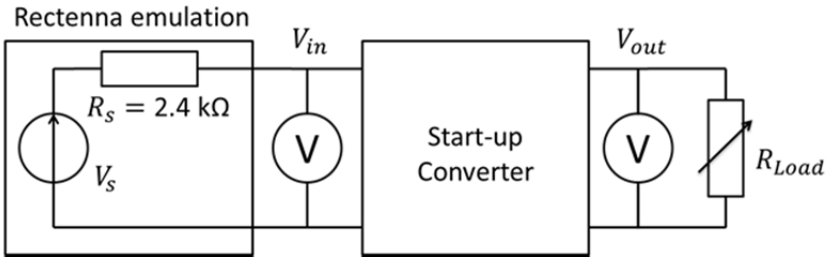

Figure 4: Experimental evaluation of the start-up converter power efficiency, $\eta_{start-up}$.

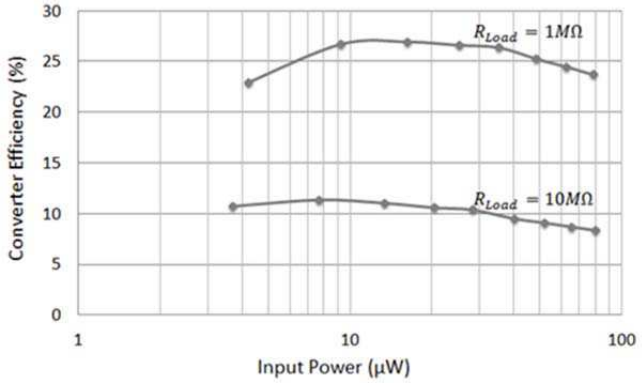

Figure 5: Experimental start-up converter efficiency vs. input power

The efficiency is around 25% and 10% for 1 MΩ and 10 MΩ resistive loads respectively. Losses are mainly due the JFET channel resistance, which is modulated by a quasi-sine signal resulting in high conduction losses. One can note from (2) that the start-up converter has an inherent compromise between steady state efficiency and start-up voltage. In fact, (2) shows that for a given source impedance and transformer turn ratio, minimizing $V_{start-up}$ (which is targeted here) requires to minimize I_{DSS}, which will, by consequence, increases the conduction losses. The efficiency is then limited due to this inherent characteristic of the Armstrong oscillator. The use of this converter will then be restrained to the start-up phase where a high voltage level is needed to launch the high efficiency principal converter.
The start-up converter is now tested using an actual 3.9 kΩ source impedance rectenna. The RF power is injected at the input of the rectifier using a RF power source (at 2.36 GHz). The start-up converter is then powered by the rectenna and a 1 MΩ resistive load is used. The input RF power is swept from 25µW (-16 dBm) to 1 mW (0 dBm). Figure 6 shows the converter input and output voltages and the voltage step-up ratio. While the input voltage is almost always under 1 V level, the output one increases to near 8 V at 0 dBm. The voltage step-up ratio varies from 5 to 10. Experimental tests show that the achievable minimal start-up voltage is around 100 mV (equivalent to 200 mV open-circuit voltage) which corresponds to 3.7 µW of source power.

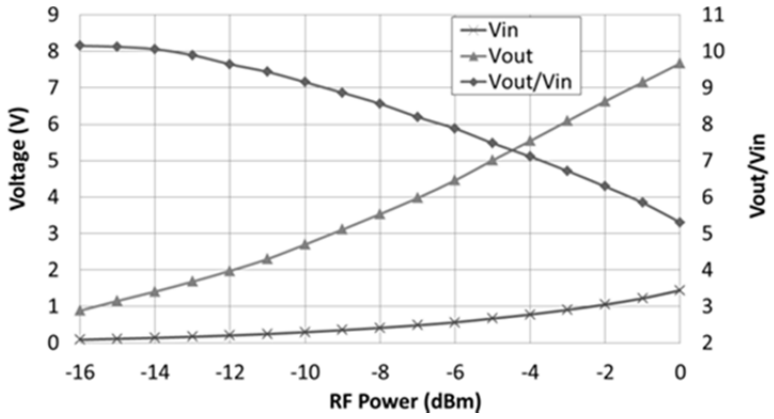

Figure 6: The start-up converter powered by a rectenna: converter input and output voltages vs. rectenna input power

3. Impedance matching converter

There are various solutions used to match the impedance of an energy source [8, 9]. One suitable technique for rectenna is static resistor emulation using a power electronics converter. As the rectenna impedance is relatively constant, open-

loop low-power controller can be considered here. In this Section an inductive Flyback converter operating in discontinuous-conduction mode (DCM) and optimized for ultra-low power rectenna applications is presented.

3.1. DCM Flyback converter topology and operation

The Flyback structure and the relative theoretical important waveforms are shown in Figure 1 and Figure 8 respectively. The MOSFET, M, is controlled in open-loop by an external constant frequency (f), constant duty cycle (d_m) signal. Primary and secondary currents expressions are given by (4) and (5) respectively.

$$i_m(t) = \begin{cases} \frac{V_{in}}{L_m} t, & 0 < t < d_m T \\ 0, & else \end{cases} \tag{4}$$

$$i_d(t) = \begin{cases} -\frac{V_{out}}{L_d}\, t + i_{d\_max}, & d_m T < t < (d_m + d_d)T \\ 0, & else \end{cases} \tag{5}$$

Where L_m and L_d are the primary and secondary flyback inductances respectively and T the period of the control signal. The other parameters are given at Figure 1 and Figure 7.
Supposing DCM operation, the Flyback input impedance can be calculated as:

$$R_{in} = \frac{V_{in}}{i_{m\_AVG}} = \frac{V_{in}}{\frac{1}{T}\int_0^{d_m T} i_m(t)\, dt} = \frac{V_{in}}{\frac{V_{in}\, d_m^2\, T}{2L_m}} = \frac{2L_m f}{d_m^2} \tag{6}$$

Supposing a perfect impedance matching between the rectenna and the flyback converter, i.e., $R_{in} = R_s$ or $V_{in} = V_s/2$, the maximal theoretical source power is given by:

$$P_{s\_\mathrm{MAX}} = \frac{{V_{in}}^2}{R_{in}} = \frac{(\frac{V_s}{2})^2}{R_s} = \frac{V_s^2}{4R_s} \tag{7}$$

The duty cycle d_d relative to the diode conduction phase can be expressed as function of d_m by considering that the average voltage across L_m during a period is null (Fig. 8), i.e. $d_m V_{in} = d_d(V_{out} \backslash m)$. This gives the following relation:

$$\frac{d_d}{d_m} = m\frac{V_{in}}{V_{out}} = m\frac{V_s}{2V_{out}} \tag{8}$$

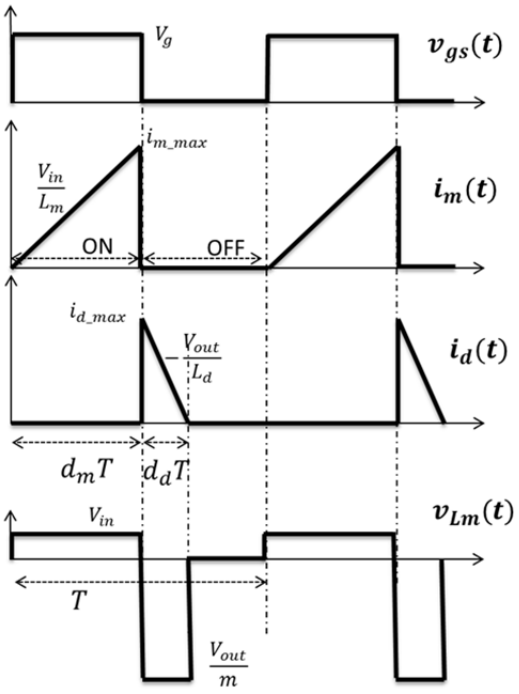

Figure 7: Schematic DCM Flyback converter waveforms for a constant switching frequency

Using previous relations and supposing perfect impedance matching, average (AVG), maximum (MAX) and RMS values of i_m and i_d can be calculated (Table I).

TABLE I

AVERAGE, MAXIMUM AND RMS² EXPRESSIONS OF THE MOSFET AND THE DIODE CURRENTS (i_m AND i_d)

Values	i_m	i_d
AVG	$\frac{V_s}{2R_s}$	$\frac{V_s^2}{4V_{out}R_s}$
MAX	$\frac{V_s}{d_m R_s}$	$\frac{V_s}{m\, d_m R_s}$
RMS^2	$\frac{V_s^2}{3d_m R_s^2}$	$\frac{V_s^3}{6\, m\, d_m R_s^2 V_{out}}$

Loss overhead

As the UVLO represents a high impedance load for the flyback converter, V_{out} will be considerably high as regard to V_s. For this reason the turn-ratio, m, will be unity as the flyback structure operating in DCM steps-up sufficiently the input voltage. These assumptions are considered for loss calculation. Also, impedance matching conditions are considered here, i.e. $R_{in} = R_s$ and $V_{in} = V_s/2$.

Conduction losses

The conductions losses in the MOSFET are due to the current flow through the channel drain-source resistance $R_{ds(on)}$ during the on-state. Furthermore the high-level voltage applied to the MOSFET gate V_g is used as a parameter in the optimization process. The MOSFET conduction losses P_{cnd_Mos} are given by:

$$P_{cnd\_Mos} = R_{ds(on)}(V_g).\ {i_{m\,RMS}}^2 = R_{ds(on)}(V_g).\ \frac{V_s^2}{3d_m R_s^2} \tag{9}$$

During the diode conduction phase, conduction losses are due to the diode forward voltage V_d. These losses can then be evaluated as:

$$P_{cnd\_d} = V_d.\, i_{d\,AVG} = \frac{V_d\, V_s^2}{4V_{out}R_s} \tag{10}$$

Losses due to diode reverse current should also be taken into account. They appear when the diode is reverse-biased (Figure 7) and are then given by:

$$P_{rev\_d} = I_{rev\_d}.\left[d_m\left(m\frac{V_s}{2} + V_{out}\right) + (1 - d_m - d_d)V_{out}\right] \approx I_{rev\_d}.V_{out} \tag{11}$$

Where I_{rev_d} is the diode reverse current which depends on V_d.
The coupled-inductances conduction losses are due to the resistive parts of the primary and secondary inductances (R_{Lm} and R_{Ld}); they are given by:

$$P_{cnd\_ind} = R_{Lm}{i_{m\,RMS}}^2 + R_{Ld}\ {i_{d\,RMS}}^2 = (R_{Lm} + \frac{V_s}{2mV_{out}}R_{Ld})\frac{V_s^2}{3d_m R_s^2} \tag{12}$$

In this realization, it has been calculated that the coupled-inductances magnetic core loss can be neglected as the selected core never get saturated for the power levels under consideration.

Switching losses

There are two kinds of MOSFET switching losses during the channel switching-off event. The first one is due to the time delay of the channel to switch-off. During this short period (t_{OFF}) the product of the drain-source voltage v_{ds} and the drain-source current i_m is not null. In fact, there is a triangle formed by the variation of i_m from i_{m_MAX} to 0 and the variation of v_{ds} from 0 to its maximum value: $v_{ds\_MAX} = V_{in} + V_{out}/m$. The expression of these switching losses is given by:

$$P_{sw\_toff} = \frac{1}{2}t_{OFF}\left(V_{in} + \frac{V_{out}}{m}\right)i_{m\,MAX}.f = \frac{1}{2}t_{OFF}\left(\frac{V_s}{2} + \frac{V_{out}}{m}\right)\frac{V_s}{d_m R_s}f \approx \frac{1}{2}t_{OFF}\frac{V_s V_{out}}{d_m R_s}f \tag{13}$$

The second kind of MOSFET switching losses is caused by the drain-source stray capacitor C_{oss}. During the channel switch-off event, this capacitor is charged from 0 to v_{ds_MAX}. The expression of these losses is given by:

$$P_{sw\_Coss} = \frac{1}{2} C_{oss} \left(\frac{V_s}{2} + \frac{V_{out}}{m} \right)^2 . f \approx \frac{1}{2} C_{oss} {V_{out}}^2 . f \tag{14}$$

At the diode level there is the same kind of phenomenon which happen during the diode switching-off event. The diode junction capacitor C_j is then charged from 0 to $mV_{in} + V_{out}$. The expression of P_{sw_Cj} is given by:

$$P_{sw\_Cj} = \frac{1}{2} C_j \left(m \frac{V_s}{2} + V_{out} \right)^2 . f \approx \frac{1}{2} C_j {V_{out}}^2 . f \tag{15}$$

Controller losses

The consumption of the controller circuit can be expressed as the product of its supply voltage level V_g by the quiescent current i_{ctrl_Q} drawn from the power supply.

$$P_{ctrl\_Q} = V_g . i_{ctrl\_Q} \tag{16}$$

This expression considers only the controller quiescent consumption; the MOSFET driver requirements will be considered separately.
As the controller drive the MOSFET gate, there are switching losses due to the total gate charge Q_g which depends on the gate voltage V_g. Driver losses due to Q_g are expressed using the gate equivalent capacitor $C_{gin} = Q_g / V_g$ and they are given by:

$$P_{Driv} = Q_g V_g f = C_{gin} {V_g}^2 f \tag{17}$$

3.2. Efficiency definition

Two expressions of the converter efficiency are considered: η_{Fly_Only} for which only internal converter loss are considered and η_{Fly_Glob} for which controller losses $P_{Ctrl} = P_{ctrl\_Q} + P_{Driv}$ are included.

$$\eta_{Fly\_Only} = \frac{P_{Fly\_in} - (P_{Mos} + P_{Diode} + P_{Ind})}{P_{Fly\_in}} \tag{18}$$

$$\eta_{Fly\_Glob} = \frac{P_{Fly\_in} - (P_{Mos} + P_{Diode} + P_{Ind} + P_{Ctrl})}{P_{Fly\_in}} \tag{19}$$

Where $P_{Mos} = P_{cnd\_Mos} + P_{sw\_toff} + P_{sw\_Coss}$, $P_{Diode} = P_{cnd\_d} + P_{sw\_Cj} + P_{rev\_d}$ and $P_{Ind} = P_{cnd\_ind}$.

3.3. Design of the flyback converter

Based on the low-current rectenna characteristics, the selected MOSFET is the FDV301N and the diode is the HSMS2822 device. Table II depicts main devices' parameters. As the diode is most of the time reverse-biased, the low value of $I_{rev\_d} < 30\ nA$, will contribute in the reduction of conduction losses.

TABLE II

SELECTED MOSFET AND SCHOTTKY DIODE FOR THE FLYBACK CONVERTER

Symbol	Description	Value	Unit
	MOSFET (FDV301N)		
$R_{ds(on)}$	Drain-source On-resistance @ $V_{gs} = 2.7\ V$	5	Ω
V_{th}	Threshold voltage	0.7-1.02	V
C_{in}	Gate equivalent input capacitance	100	pF
C_{oss}	Output capacitance	6	pF
	DIODE (HSMS2822)		
V_d	Forward voltage @ 100 µA	240	mV
C_j	Junction Capacitance	0.7	pF
I_{rev_d}	Reverse current @ $V_d = -2.5\ V$	< 30	nA

The efficiency and the primary inductance L_m (from (6)) have been evaluated as function of the switching frequency, f (Figure 8). One can observe that switching frequency impacts considerably on the global efficiency especially at low power levels. Gate driving represents the most important contribution in switching losses. A switching frequency, $f = 10\,kHz$, and an inductance value, $L_m = 30\,mH$, has been selected in order to obtain a correct efficiency at µW levels.

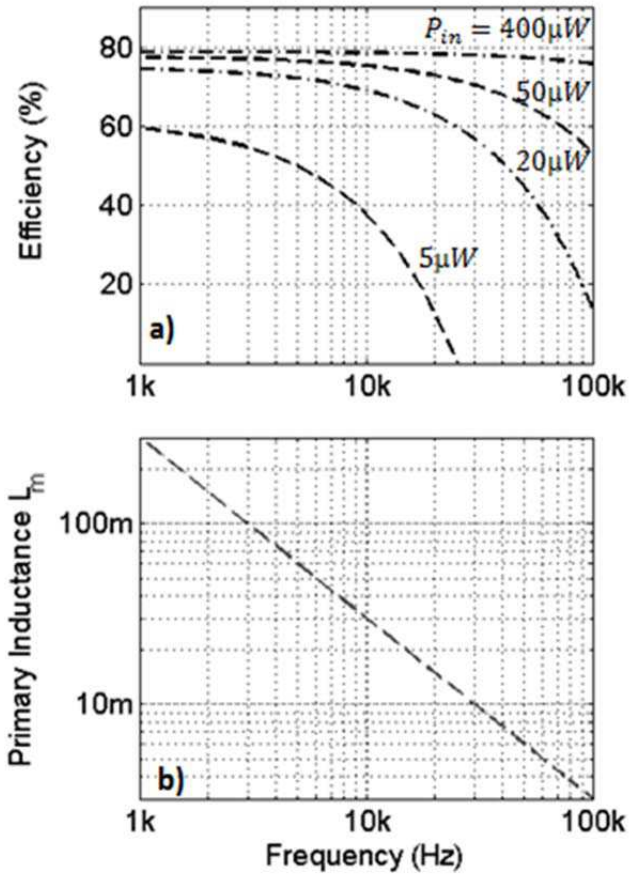

Figure 8: Calculated global flyback converter efficiency, η_{Fly_Glob}, and primary inductance, L_m, as function of the switching frequency f ($d_m = 0.5$).

Figure 9 shows calculated efficiency as function of controller supply voltage, V_g. One can observe that $1.2\,V$ is a good trade-off between conduction and switching losses.

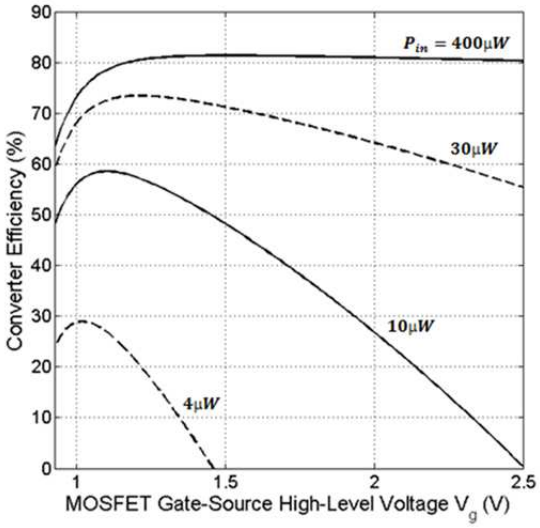

Figure 9: Calculated global flyback converter efficiency, η_{Fly_Glob}, as function of the controller supply voltage V_g. Parameters: f = 10kHz, dm = 0.5 and Lm = 30 mH.

The turn-ratio, m, is unity as the flyback structure operating in DCM steps-up sufficiently the input voltage. Moreover, when the converter output voltage is high with regard to the input one, the secondary winding conduction time $d_d T$ is very short as regard to the primary winding one $d_m T$ as shown by (8). As a consequence, the designed coupled inductances should have a broadband frequency capability in order to avoid current distortions and then additional losses. A prototype was fabricated and tested. The selected magnetic is a compact (20mm x 10mm x 6mm) double E ferrite core with a broad-band frequency (>100 kHz for the final coupled-inductances).
The controller is a TS3001 commercial integrated circuit oscillator. When it drives the FDV301N switch (at $f = 10\ kHz$) it consumes 1.44 µW power under 1.2 V supply voltage.

3.4. Experimental results

Experimental tests in anechoic chamber are realized as detailed at Figure 10. A 2.45 GHz RF source coupled to a horn antenna (gain $G_{emit} = 20\ dBi$) are used for the transmission side. At the receiver side a rectifier coupled to a compact antenna (gain $G_{recv} = 6\ dBi$) are used (Section II). The transmission distance is $d = 1\ m$. The Flyback converter is powered by the rectenna and a 200 kΩ resistive load is placed at its output. The controller is powered by an auxiliary power source $V_g = 1.2\ V$.
The received RF power at the rectifier input can be evaluated using the Friis equation [10] as follow:

$$P_{recv}(dBm) = P_{emit}(dBm) + G_{emit}(dBi) + G_{recv}(dBi) - 20\log\left(\frac{4\pi d}{\lambda}\right) = P_{emit}(dBm) - 22\ dB \tag{20}$$

Where λ is the wave length relative to the 2.45 GHz RF signal.

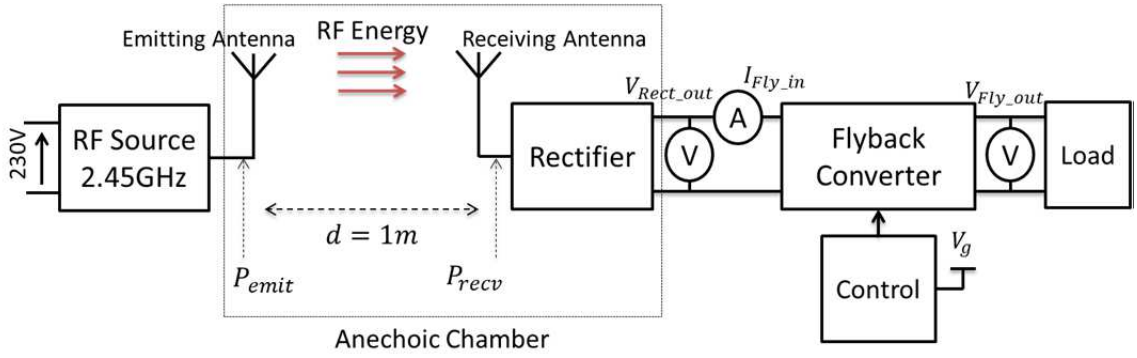

Figure 10: Experimental anechoic chamber test of the flyback converter

The input voltage V_{Rect_out}, input current I_{Fly_in} and output voltage V_{Fly_out} of the flyback converter are measured for different RF power levels. The efficiency of the flyback converter alone η_{Fly_Only}, and the efficiency of the flyback converter including the controller, η_{Fly_Glob}, are then evaluated as follow:

$$\eta_{Fly\_Only} = \frac{P_{Load}}{P_{Fly\_in}} = \frac{\frac{V_{Fly\_out}^2}{R_{Load}}}{I_{Fly\_in}\, V_{Rect\_out}} \tag{21}$$

$$\eta_{Fly\_Glob} = \frac{P_{Load} - P_{Ctrl}}{P_{Fly\_in}} = \frac{\frac{V_{Fly\_out}^2}{R_{Load}} - 1.44\ \mu W}{I_{Fly\_in}\, V_{Rect\_out}} \tag{22}$$

Figure 11 shows the voltage delivered by the rectenna, V_{Rect_out}, and the one delivered by the flyback converter, V_{Fly_out}, as function of the RF received power P_{recv}. Though V_{Rect_out} is limited to 250 mV, the flyback output voltage V_{Fly_out} reaches 1 V at -15 dBm and 2.5 V at -10 dBm, which corresponds to a voltage step-up ration of 10.

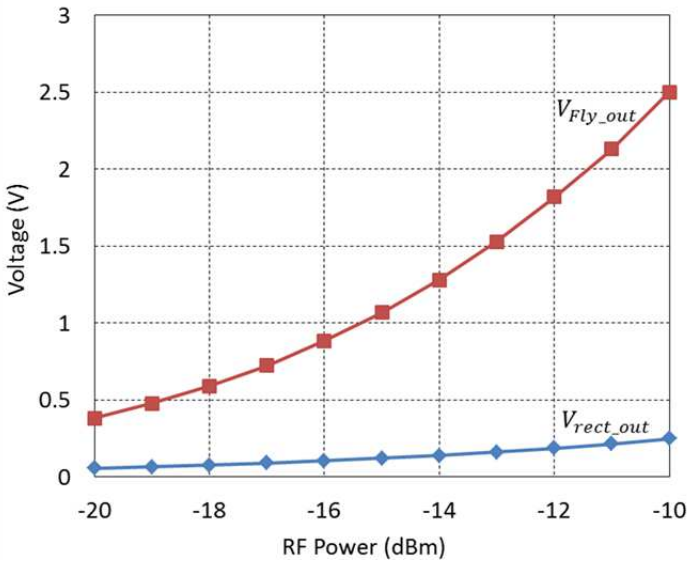

Figure 11: Flyback converter input and output voltages as function of the RF power P_{recv} ($R_{Load} = 200\ k\Omega$.).

Figure 12 shows the efficiencies of the flyback converter. The converter global efficiency η_{Fly_Glob} including controller consumption is over 50% at -15 dBm and reaches 75% at -10 dBm.

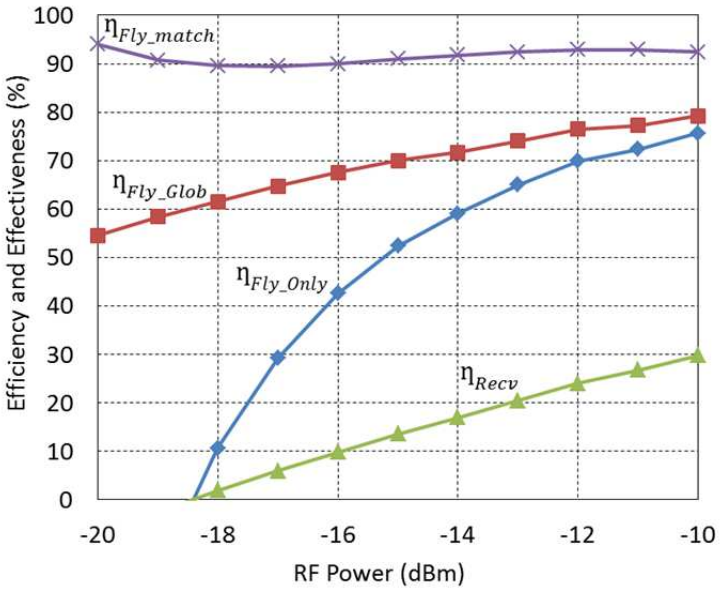

Figure 12: Efficiencies and impedance matching effectiveness as function of the received RF power P_{recv}

The rectenna output power, P_{rect_max}, with a 1600 Ω has been evaluated separately. We define the impedance matching effectiveness, η_{Fly_match} and the global receiver efficiency, η_{Recv}, as follow:

$$\eta_{Fly\_match} = \frac{P_{rect\_out}}{P_{rect\_max}} = \frac{V_{rect\_out} \cdot I_{Fly\_in}}{P_{rect\_max}} \tag{23}$$

$$\eta_{Recv} = \frac{P_{Load} - P_{Ctrl}}{P_{recv}} = \frac{\frac{V_{Fly\_out}^2}{R_{Load}} - 1.44\ \mu W}{P_{recv}} \tag{24}$$

The impedance matching using the flyback converter shows excellent effectiveness, i.e. more than 89%. Separate tests using a constant resistance source shows an effectiveness superior to 99%. The receiver is operational from -18 dBm of RF received power and reaches a global PCE of 30% at 0 dBm.

4. Complete System

The objective of this part is to present a system which allows a coordinated operation between the start-up and the flyback converters toward an autonomous power supply.

In [5] a low power UVLO circuit uses two comparators in order to set a lower and an upper threshold voltages is presented. The circuit proposed here uses MOSFETs rather than comparators to set the threshold voltages (Figure 1). A P-channel MOSFET associated with the resistor, R_p, is used as a switch between the input and the output ports of the UVLO. A diode D_{hold} and a capacitor C_{hold} are added in order to stabilize the gate-source voltage of NMOS1.
Once the output capacitor reaches the high voltage limit, the UVLO connects the capacitor to the output load. The switch NMOS2 allows to keep the PMOS in on state till the low voltage limit is reached. Experimental tests of the UVLO with the start-up converter are shown at Figure 13.

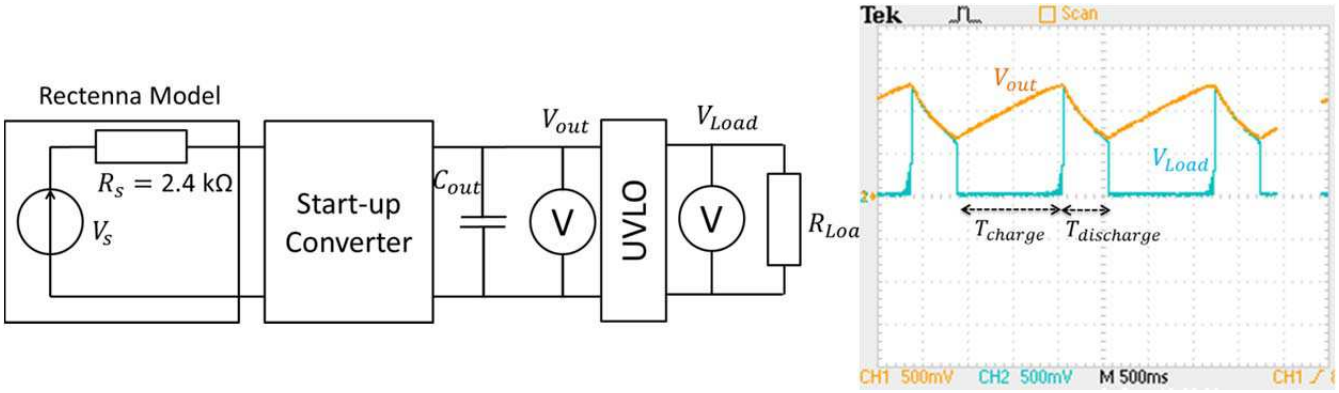

Figure 13: Experimental tests: UVLO input and output voltages with: NMOS1/2 = FDV301N, PMOS = FDV304P, R1 = 25 MΩ, R2 = 10 MΩ, Rp = 10 MΩ, Vs = 800 mV, Rs = 2.4 kΩ, Cout = 4.7 µF and RLoad = 100 kΩ.

Measurements show that high and low limit voltages are 1.3 V and 0.65 V respectively. The load operation time is lower than the charging time of C_{out} (0.5 s and 2.2 s respectively), which means that the source power level is inferior to the power needed by the load.
Now we present a structure which will permit us to connect both converters in order to work with the start-up converter at the beginning and then with the flyback converter as the main converter (Figure 14).

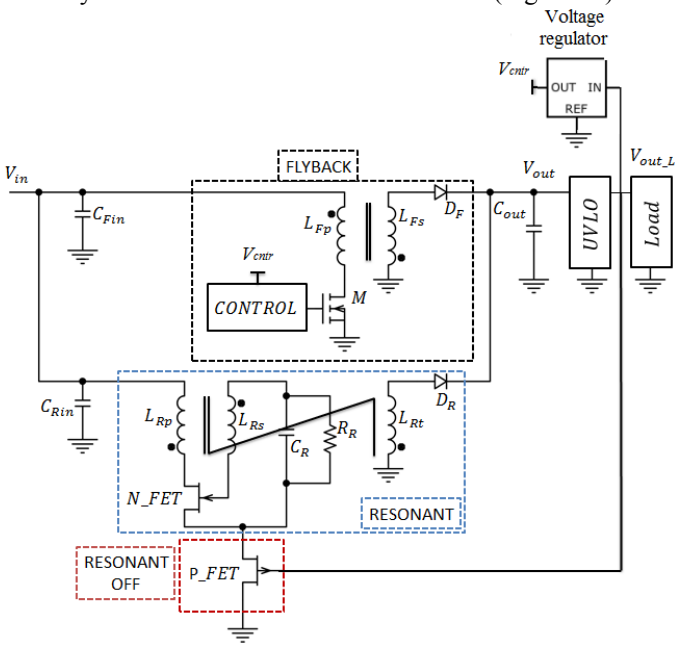

Figure 14: Coupling structure

Figure 15: at the first moment, the capacitor C_{out} is empty, so the UVLO output voltage V_{out_L} is null and the start-up converter is working. Along the time the capacitor C_{out} will be charged until it arrives to V_{high} voltage, when the UVLO will close its circuit and V_{out_L} will have the same value that V_{out}.

At this moment, two factors come into play. On one hand, the P-JFET Normally-on has a positive voltage, $V_{gs} > V_{th\_PJFET}$, so it will open the start-up circuit. On other hand, the input voltage of the controller will be obtained after reduce V_{out_L} by the voltage regulator. In this way, we will guarantee that the oscillator will work in its correct working voltage and it will be able to start the flyback converter. Thereafter, it will be self-powered by the main converter.

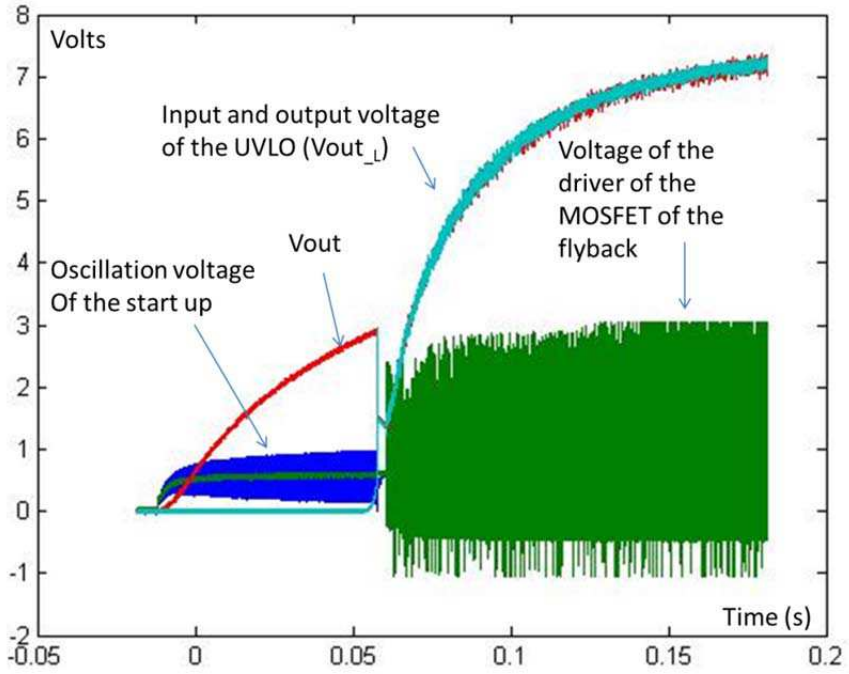

Figure 15: Voltages in the complete circuit (Rlaod = 200 kΩ)

5. Conclusion

In this paper, a complete power management system for RF energy harvesting in WPT scheme was presented. The system is composed by two main elements: a start-up and a flyback converter. The presented start-up converter based on the Armstrong oscillator achieves cold start-up as low as 100 mV (200 mV open circuit) at ultra-low power (3.7 µW). The flyback converter operating in DCM achieves a conversion efficiency over 50% at 9 µW and a peak efficiency of 84% at 370 µW, with an impedance matching effectiveness over 89%. Finally, an UVLO circuit is proposed to manage the operation of the load as function of the available power from the source.

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